AMENDMENTS TO THE CLAIMS

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1. (original) A microprocessor, comprising:

a microcode unit for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:

an instruction address input for receiving an instruction address;

a control variable input for receiving a control variable corresponding to a current state of the microprocessor;

a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; and

a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit.

2. (original) The microprocessor according to claim 1, wherein each of the embedded logic circuits includes:

a table for performing a table lookup in response to a received instruction; and

a controller responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup for controllably setting each of the control signals required by the microprocessor for executing said received instruction.

3. (original) The microprocessor of claim 2, wherein the controller includes:

means for setting a control signal to a "1" regardless of its immediately preceding value;

means for setting a control signal to "0" regardless of its immediately preceding value; and

means for not modifying a control signal from its immediately preceding value.

4. (original) The microprocessor of claim 3, wherein the controller further includes:

means for setting a control signal to a data state.

5. (canceled)

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6. (currently amended) The ~~method~~ microprocessor according to claim 1, further comprising means for determining which of the control signals are not to be modified for each instruction.

7-8. (canceled)

9. (original) A microcode unit in a microprocessor, for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:

an instruction address input for receiving an instruction address;

a control variable input for receiving a control variable corresponding to a current state of the microprocessor;

a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; and

a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit.

10-19. (canceled)

20. (original) A method of providing a state machine decoding, comprising:

decoding a current opcode to provide a decode;

setting required functions signals;

setting exclusive functions outside of the current opcode to a previous state; and

latching results of the decode.

21-22. (canceled)